METHOD AND APPARATUS FOR CONTROLLING A PROCESSOR IN A DATA PROCESSING SYSTEM

ABSTRACT

Method and apparatus for controlling a processor in a data processing system is described. In an example, the processor is maintained in a halt condition in response to reset information received from the data processing system (200) (e.g., initialization of an integrated circuit having a processor embedded therein). At least one memory resource in communication with the processor is configured. The processor is then released from the halt condition.